

PATENT ABSTRACTS OF JAPAN

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(71)Applicant : NEC CORP

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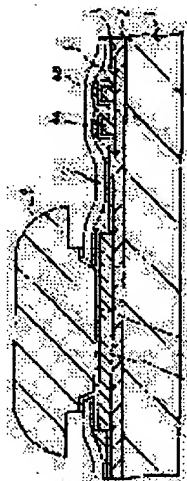
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(54) SEMICONDUCTOR DEVICE

(57)Abstract:

PURPOSE: To obtain a highly reliable semiconductor device wherein etching resistance and humidity resistance are improved, by constituting a protecting insulative film formed to be on the periphery of a metal pad and on a metal wiring, of a first insulative film formed by CVD method, a second insulating film formed by spin-coating method, and a third insulative film formed by CVD method.

CONSTITUTION: On a semiconductor substrate 1, an Al pad 3 and Al wirings 4A, 4B are formed, via an interlayer insulative film 2 composed of a silicon oxide film and the like. On the periphery of the Al pad 3 and on the Al wirings 4A, 4B, a passivation film composed of a three-layered insulative film is formed. That is, said passivation film is constituted of a first insulative film 5 composed of silicon oxide film formed by normal pressure or reduced pressure CVD method, a second insulative film 6 composed of a silicon oxide film formed by spin-coating method, and a third insulative film 7 composed of silicon nitride film formed by plasma CVD method.



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(54) Title of the Invention:

SEMICONDUCTOR DEVICE

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Specification

Title of the Invention:

SEMOCONDUCTOR DEVICE

Scope of Claims:

A semiconductor device, wherein, in a semiconductor device that has a metal pad and metal wiring formed on a semiconductor substrate via an interlayer insulation film, a protective insulation film that is formed around the periphery of the metal pad and on the metal wiring, and a protrusion electrode formed on the metal pad via a metal layer for a barrier, the protective insulation film is comprised of a 1st insulation film formed using a CVD method, a 2nd insulation film formed using a spin-coating method and a 3rd insulation film formed using the CVD method, which all are formed consecutively.

Detailed Explanation of the Invention:

[Industrial Application]

The present invention relates to a semiconductor device, and relates in particular to a structure of a protective insulation film in the semiconductor device that has a protrusion electrode for gang bonding.

[Prior Art]

Conventionally, this type of semiconductor device has had the structure shown in Fig. 2.

In Fig. 2, '1' is a semiconductor substrate, '2' is an interlayer insulation film, '3' is an Al pad for the extraction to outside, and '4A' and '4B' are internal Al wiring formed at a minimum interval. Then, a protective insulation film (hereafter referred to as a 'passivation film') formed on the Al wiring 4A and 4B and around the periphery of the Al pad 3 is a two-layer structure comprised of an silicon oxide film 10 with 0.5 – 1.0 μm of a thickness formed using the CVD method at normal pressure or a low pressure and a nitride film 11 with 0.2 – 1.0 μm of thickness formed using a plasma CVD method where there are fewer pinholes.

Then, a protrusion electrode (hereafter referred to as a 'bump') 9 is formed in the center of the Al pad via a barrier metal 8. At this time, the barrier metal 8 is formed with a film that has two or more layers, such as titanium – palladium, titanium – platinum, titanium – copper – gold, or chrome – copper – gold, and the bump is formed with a material, such as gold, copper or solder.

[Problems Overcome by the Invention]

However, in the passivation film in the above-mentioned conventional semiconductor device, a concave portion 12 or/and a hollow portion 13 is/are easily formed in between the Al wiring 4A and 4B, and in the case that the bump 9 is formed in the posterior process and the barrier metal 8 is removed by etching, the regions where these concave portion 12 and hollow portion 13 have been formed are weak with respect to the etching, so that there is a defect of the Al wiring 4A & 4B under the regions also becoming etched. Further, even in the case that the Al wiring are not etched, moisture resistance becomes deteriorated due to pinhole(s), with the problem of decreased reliability.

The objective of the present invention is to provide a semiconductor device with high reliability that has a passivation film where the etching resistance and the moisture resistance are improved.

[Problem Resolution Means]

Concerning the semiconductor device of the present invention, in a semiconductor device that has a metal pad and metal wiring, formed on a semiconductor substrate via an interlayer insulation film, a protective insulation film formed around the periphery of the above-mentioned metal pad and on the above-mentioned metal wiring, and a protrusion electrode formed on the above-mentioned metal pad via a metal layer for a barrier,

the above-mentioned protective insulation film is comprised of a 1st insulation film formed using a CVD method, a 2nd insulation film formed using a spin-coating method and a 3rd insulation film formed using the CVD method, which all are formed consecutively.

[Embodiment]

An embodiment of the present invention is explained hereafter, with reference to the drawings.

Fig. 1 is a cross-sectional view of an embodiment for the present invention.

In Fig. 1, the Al pad 3 and the Al wiring 4A & 4B are formed on the semiconductor substrate 1 via the interlayer insulation film 2 comprised of silicon oxide generally. Then, a passivation film comprised of a three-layer insulation film is formed around the periphery of the Al pad 3 and on the Al wiring 4A & 4B.

Specifically, the passivation film is constructed with a 1st insulation film comprised of a silicon oxide film, which has 0.1 – 0.3 μm of thickness and is formed using the CVD method under a normal pressure or a low pressure; a 2nd insulation film 6 comprised of a silicon oxide film, which has 0.3 – 0.5 μm of thickness and is formed using the spin-coating method; and a 3rd insulation film 7 comprised of a silicon nitride film, which has less pinhole(s), has approximately 0.5 μm of thickness and is formed using the plasma CVD

method. Then, the bump 9, which is comprised with gold or copper generally, is formed via the barrier metal 8, which has 0.1 – 0.5 μm of thickness and is comprised of titanium – copper or titanium – gold generally.

In the present embodiment constructed as mentioned above, since the passivation film is formed with a three-layer insulation film, no hollow portion or concave portion is formed between the Al wiring 4A and 4B, because the 2nd insulation film 6 is formed using the spin-coating method. Therefore, in the case of etching the barrier metal 8 in the posterior process, the Al wiring 4A & 4B will not be etched, resulting in the improvement of moisture resistance, as well.

[Efficacy of the Invention]

As explained above, in the present invention, protective insulation film, formed around the periphery of the metal pad and on the metal wiring, is comprised of a 1st insulation film formed using the CVD method, a 2nd insulation film formed using the spin-coating method and a 3rd insulation film formed using the CVD method, resulting in the improvement of the etching resistance and moisture resistance, so that a semiconductor device that has a high reliability can be obtained.

Brief Explanation of Drawings:

Fig. 1 is a cross-sectional view of an embodiment of the present invention, and Fig. 2 is a cross-sectional view of a conventional semiconductor device.

1 ... semiconductor substrate, 2 ... interlayer insulation film, 3 ... Al pad, 4A & 4B ... Al wiring, 5 ... 1st insulation film, 6 ... 2nd insulation film, 7 ... 3rd insulation film, 8 ... barrier metal, 9 ... bump, 10 ... silicon oxide film, 11 ... nitride film, 12 ... concave portion, 13 ... hollow portion

Agent: Patent agent: Shin UCHIHARA

- | | |
|-------------------------------|------------------------------------|
| 1: Semiconductor substrate | 5: 1 st insulation film |
| 2: Interlayer insulation film | 6: 2 nd insulation film |
| 3: Al pad | 7: 3 rd insulation film |
| 4A & 4B: Al wiring | 8: Barrier metal |

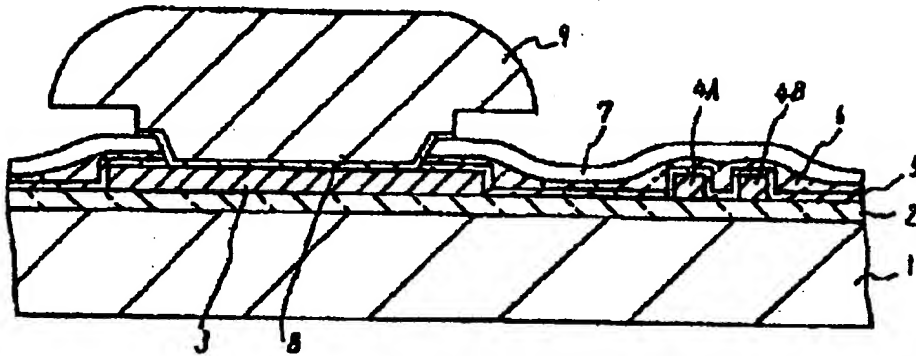


FIG. 1

- | | |
|------------------------|---------------------|
| 9: Bump | 12: Concave portion |
| 10: Silicon oxide film | 13: Hollow portion |
| 11: Nitride film | |

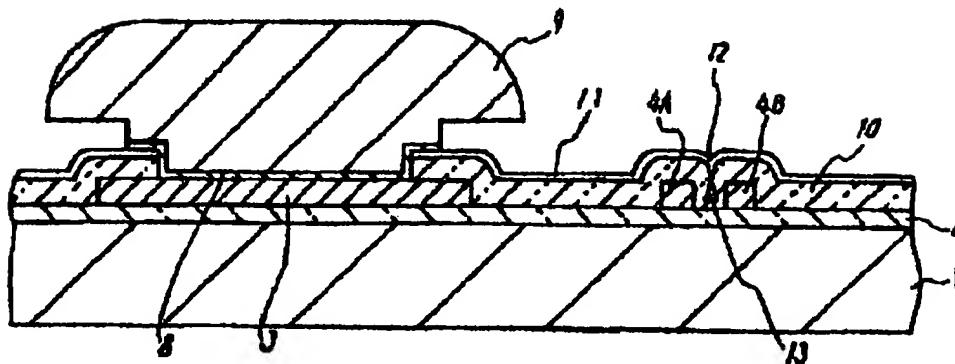


FIG. 2

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⑪ 特許出願公開

⑫ 公開特許公報(A) 平2-21622

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審査請求 未請求 請求項の数 1 (全3頁)

⑮ 発明の名称 半導体装置

⑯ 特 願 昭63-170623

⑰ 出 願 昭63(1988)7月8日

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明 細 書

発明の名称

半導体装置

特許請求の範囲

半導体基板上に層間絶縁膜を介して形成された金属パッドと金属配線と、前記金属パッドの周辺部上および前記金属配線上に形成された保護用絶縁膜と、前記金属パッド上にバリア用の金属層を介して形成された突起電極を有する半導体装置において、前記保護用絶縁膜は順次形成されたCVD法による第1の絶縁膜と回転塗布法による第2の絶縁膜とCVD法による第3の絶縁膜とから構成されていることを特徴とする半導体装置。

発明の詳細な説明

(産業上の利用分野)

本発明は半導体装置に関し、特にギャングボンディング用の突起電極を有する半導体装置の保護

用絶縁膜の構造に関する。

(従来の技術)

従来、この種の半導体装置は、第2図に示すような構造を有していた。

第2図において、1は半導体基板、2は層間絶縁膜、3は外部引き出し用のA₁パッド、4A、4Bは最小間隔で形成された内部のA₁配線である。そして、これらA₁配線4A、4B上およびA₁パッド3の周辺上に形成される保護用絶縁膜(以下パッシベーション膜という)は、常圧もしくは低圧のCVD法による厚さ0.5~1.0μmの酸化シリコン膜10とピンホールの少ないプラズマCVD法による厚さ0.2~1.0μmの窒化膜11の2層構造となっていた。

そして、A₁パッド中央部にはバリア金属8を介して突起電極(以下バンパという)9が形成されている。この時バリア金属8はチタン-パラジウム、チタン-白金、チタン-銅-金、クロム-銅-金などの2層以上の膜で形成され、バンパは金、銅、半田などの材料で形成される。

〔発明が解決しようとする課題〕

しかしながら、上述した従来の半導体装置におけるパッシベーション膜は、A₁配線4A、4B間に凹部12や空洞部13が形成されやすく、後工程でパンプ9の形成を行ない、バリアメタル8をエッチングによって除去する場合、これら凹部12や空洞部13の形成された領域がエッチングに対して弱く、下のA₁配線4A、4Bまでエッチングされるという欠点があった。また、A₁配線がエッチングされない場合でもピンホールのため耐湿性が劣化し、信頼性が低下するという問題点があった。

本発明の目的は、耐エッチング性および耐湿性の向上したパッシベーション膜を有する信頼性の高い半導体装置を提供することにある。

〔課題を解決するための手段〕

本発明の半導体装置は、半導体基板上に層間絶縁膜を介して形成された金属パッドと金属配線と、前記金属パッドの周辺部上および前記金属配線上に形成された保護用絶縁膜と、前記金属パ

ッドからなる第2の絶縁膜6と、ピンホールの少ないプラズマCVD法による厚さ約0.5 μ mの窒化シリコン膜からなる第3の絶縁膜7とから構成されている。そして、A₁パッド3の中央部には、厚さ0.1～0.5 μ mのチタン-銅、チタン-金等からなるバリアメタル8を介して金や銅等からなるパンプ9が形成されている。

このように構成された本実施例においては、パッシベーション膜が3層の絶縁膜で形成されているため、特に第2の絶縁膜6が回転塗布法により形成されていることにより、A₁配線4A、4B間に空洞部や凹部が形成されることはなくなる。従って、後工程においてバリアメタル8をエッチングした場合でも、A₁配線4A、4Bがエッチングされることはなくなり、耐湿性も向上したものとされる。

〔発明の効果〕

以上説明したように本発明は、金属パッドの周辺部上および金属配線上に形成される保護用絶縁膜を、CVD法による第1の絶縁膜と回転塗布法

ド上にバリア用の金属層を介して形成された突起電極を有する半導体装置において、前記保護用絶縁膜は順次形成されたCVD法による第1の絶縁膜と回転塗布法による第2の絶縁膜とCVD法による第3の絶縁膜とから構成されているものである。

〔実施例〕

次に、本発明の実施例について図面を参照して説明する。

第1図は本発明の一実施例の断面図である。

第1図において、半導体基板1上には、酸化シリコン膜等からなる層間絶縁膜2を介してA₁パッド3及びA₁配線4A、4Bが形成されている。そして、A₁パッド3の周辺部上及びA₁配線4A、4B上には、3層の絶縁膜からなるパッシベーション膜が形成されている。

すなわち、パッシベーション膜は、常圧または低圧CVD法による厚さ0.1～0.3 μ mの酸化シリコン膜からなる第1の絶縁膜5と、回転塗布法による厚さ0.3～0.5 μ mの酸化シリコ

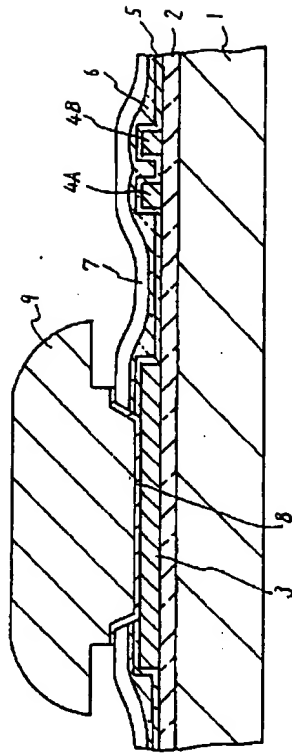
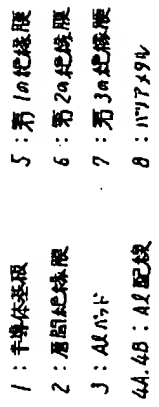
ンによる第2の絶縁膜6とCVD法による第3の絶縁膜7とで構成することにより、耐エッチング性および耐湿性が向上するため、信頼性の高い半導体装置が得られる。

図面の簡単な説明

第1図は本発明の一実施例の断面図、第2図は従来の半導体装置の断面図である。

1…半導体基板、2…層間絶縁膜、3…A₁パッド、4A、4B…A₁配線、5…第1の絶縁膜、6…第2の絶縁膜、7…第3絶縁膜、8…バリアメタル、9…パンプ、10…酸化シリコン膜、11…窒化膜、12…凹部、13…空洞部。

代理人 弁理士 内 原



圖一

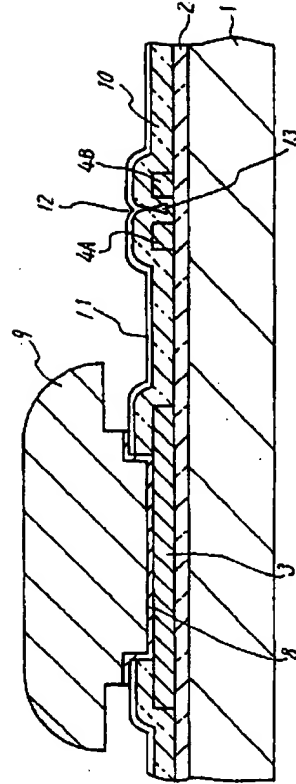
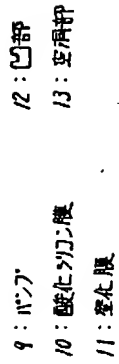


图 2